(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3302 Roll No. | | | | | | | | | | |

B.Tech.

(SEM. II) EVEN THEORY EXAMINATION 2012-13

ELECTRONICS ENGINEERING

Time : 3 Hours *Total Marks : 100*

Note :– All Sections are compulsory.

SECTION–A

1. All parts are compulsory. Write short answers by giving proper reasons : **(2×10=20)**
   (a) Find the value of DC resistance of a Germanium Junction diode at 25°C with I_0 = 25 μA and an applied voltage of 0.2 V across the diode.
   (b) Differentiate between Transition capacitance (C_T) and Diffusion capacitance (C_D) of a PN junction diode.
   (c) Draw a neat diagram of a full wave rectifier bridge circuit using Diode.
   (d) Write an expression for the ripple factor and efficiency for half wave rectifier.
   (e) The BJT has I_E = 10 mA and a = 0.98. Determine the values of I_B and β.
   (f) Sketch the input and output characteristic cure of Common Base (CB) BJT configuration.
   (g) A FET has a driven current of 4 mA if I_{DSS} = 8 mA, $V_{GS(OFF)} = -6$ V. Find the value of V_{GS} and Pinch off voltage (V_P).
   (h) Enlist the characteristics of an Ideal Op-Amp.
   (i) Realize the logic expression $F = A + BC\overline{D}$ using NAND gate only.

(j) Convert the $(6089.25)_{10\rightarrow}$ $(\ )_8$.

SECTION–B

2. Attempt any **three** parts of the following : **(10×3=30)**

(a) Draw a neat diagram of Zener voltage regulator circuit and determine the load resistance (R_L) and range of series resistance (R) value to meet the following specification : Output Voltage (V_{out}) = 5 V, Load Current (I_L) = 10 mA, Zener maximum wattage = 400 mW and Input Voltage (V_{in}) = 10 ± 2V.

(b) Draw a neat diagram and explain the working of a Center tap type full wave rectifier. Calculate the value of capacitance to use as a shunt capacitor filter in full wave rectifier with the given specification : Operating frequency 50 Hz, ripple factor 10% and load resistance is 1 kΩ.

(c) For voltage divider common source JFET configuration as shown in Figure 1, if $V_D = 12$ V and $V_{GSQ} = -2$V, determine the value of resistance (RS) :

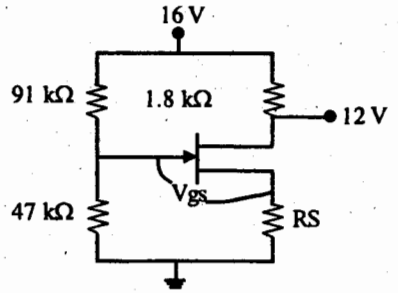

Figure 1

(d) Write an expression for small signal Hybrid model h parameters Ai, Av, Ri, Ro for CE Voltage divider bias amplifier circuit with Emitter bypass capacitor (C_E).

SECTION–C

This Section consists of 5 theory questions. Each question is of 10 marks : **(10×5=50)**

3. Attempt any **two** parts of the following : **(5×2=10)**

(a) Determine the current I as shown in Figure 2. Assume Diode is silicon diode with $V_D = 0.7$ V :

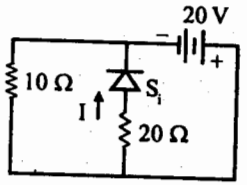

Figure 2

(b) Sketch output voltage (V_o) waveform of the following network as shown in Figure 3. Assume Diode is silicon diode with $V_D = 0.7$:

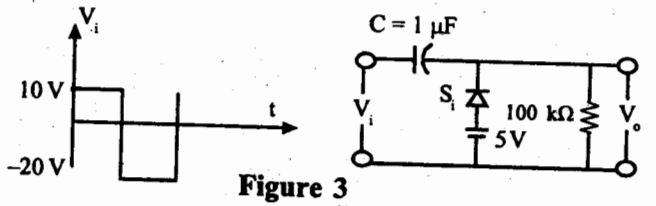

Figure 3

(c) Calculate the current I_E, I_C and I_B for the following circuit as shown in Figure 4 :

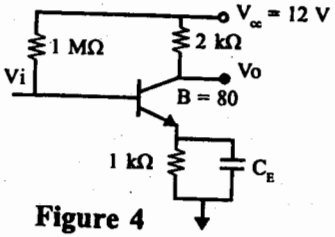

Figure 4

4. Attempt any **two** parts of the following : **(5×2=10)**

(a) Draw the neat diagram structure of JFET and explain the transfer characteristic.

(b) Explain Depletion type MOSFET with diagram and draw the transfer characteristics.

(c) Show that the trans-conductance g_m of JFET is related to drain current I_{DS} by :

$$g_m = \frac{2}{V_P}\sqrt{I_{DSS}\, I_{DS}}$$

5. Attempt any **two** parts of the following : **(5×2=10)**

(a) Draw and explain the circuit diagram for performing the Differentiator operation using Op-Amp.

(b) Derive the output voltage (V_o) for the given Figure 5 :

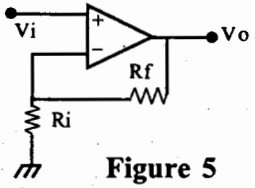

Figure 5

(c) Find the output voltage (V_o) for the given circuit as shown in Figure 6 :

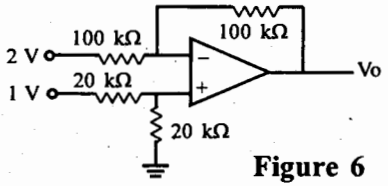

Figure 6

6. Attempt any **two** parts of the following : **(5×2=10)**

(a) (i) Write De Morgan's and Duality theorem in Digital circuits.

(ii) Simplify the Complement of the logic function

$$F = ABC + AB\overline{C} + \overline{A}\overline{B}C + \overline{A}BC .$$

(b) Simplify the following expression using K-map in Sum of Products (SOP) form.

$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$

(c) Simplify the following expression using K-map in Product of Sum (POS) form :

$F(A, B, C, D) = \Pi M(0, 1, 3, 6, 7, 8, 9, 11, 13, 14, 15)$

7. Attempt any **one** part of the following : **(10×1=10)**

(a) Using a suitable diagram explain the basic principle of a digital voltage meter.

(b) (i) Describe the working of a CRO with the help of block diagram.

(ii) Explain the measurement of phase and frequency using CRO.